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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,145	10/02/2001	Nick A. Youker	279.361US1	9584

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/970,145	YOUKER ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-13 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-02-01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 7-9, 11, 12 and 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Buckley, III, et al. (US Pat. 5477082).

Regarding claims 7, 11 and 20-25, Buckley, III, et al. disclose an electrical device (see Fig. 6) comprising:

- a flexible polyimide/tape substrate/tape automated bonding (TAB) leadframe (TABLF) substrate (see 60 in Fig. 6; Col. 3, lines 31-40; Col. 6, lines 10-13
- the TABLF including a plurality of leads/traces (see 24A/80 in Fig. 3-5), the leads/traces having a concentric generally rectangular first and second areas of the plurality of leads/traces being internally routed (see an inner area in Fig. 5; Col. 3, line 56) and configured into a generally rectangular inner lead bonding (ILB) area/portion and an outer lead bonding (OLB) area/portion (not numerically referenced in Fig. 6- see external electrodes 54 being connected to lead pads in Fig. 6; Col. 6, lines 28-31), the OLB portion having an array of external electrodes/solder balls (see 54 in Fig. 6)

- an integrated circuit (IC) chip/die having bonding pads/input-output (I/O) connections at a perimeter of the chip (see 56 and 64 in Fig. 3, 4 and 6) being connected to an exposed portion of the leads pads/leads in the ILB portion (see Fig. 4 and 6)
- the first area of the plurality of leads/traces in the ILB portion being dimensioned to directly connect respective plurality of leads/traces to the perimeter bonding pads/I-O pads (see 64 in Fig. 4; Col. 3, line 57) of the IC chip, and
- the IC chip being connected to a printed circuit card/board (PCB) by the TABLF through the lead pads/leads in the OLB portion (see the connection 50/54 in Fig. 6)

(Fig. 6; Fig. 3-7; Col. 3-7).

Buckley, III, et al. further disclose a second IC chip/electrical component (see 94 in Fig. 7) having a smaller area than that of the IC chip being mounted above/below a surface of the IC chip and electrically connected to the IC chip via respective lead pads/leads, which extend outward (24A not being numerically referenced in Fig. 7) from the second IC chip/electrical component to the perimeter bonding pads/I/O pads IC chip (see connections between 94 and 56 through 24A in Fig. 7, 6 and 3; Col. 7, lines 55-67). Such mounting configuration provides the leads/traces/pads wiring being internally routed relative to the ILB area so that the leads have respective contacts exposed (contacts on the TABLF under the second component 94 not numerically referenced in

Fig. 7- see similar terminals/contacts under bumps in Fig. 6) interior to the ILB portion of the TABLF structure above/below the major surface of the IC chip/die.

Regarding claims 8, 9 and 12, Buckley, III, et al. disclose the entire claimed structure as applied to claims 7 and 11 above, wherein Buckley, III, et al. further disclose the TABLF having a multichip module (MCM- see Fig. 6 and 7) configuration wherein two or more electrical components/chips (see 58A, 90, etc. in Fig. 6 and 7) are mounted above the IC chip (see 56 in Fig. 6) and each being electrically connected to the IC chip via respective leads/traces which extend from each of the electrical components to perimeter bonding pads/I/O pads of the IC chip (Fig. 6 and 7; Col. 7, lines 55- 67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckley, III, et al. (US Pat. 5477082) in view of admitted prior art (APA).

Regarding claims 10 and 13, Buckley, III, et al. teach substantially the entire claimed structure as applied to claims 7 and 11 above, except the IC chip being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device is dimensioned to be implantable within a body.

The APA teaches using conventional TABLF devices being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device being implantable within a body (see specification pages 1 and 2). Furthermore, determination of parameters including dimensions such as length/width, size, etc., and weight of a TAB device in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired effect/result for particular applications including medical, military, communication, etc.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC chip being adapted to monitor, regulate and control delivery of electrical impulses to a heart and the electrical device is dimensioned to be implantable within a body as taught by the APA so that the desired benefits and reliability of the device for the medical application can be achieved in Buckley, III, et al's TABLF.

Response to Arguments

5. Applicant's arguments filed on 07-11-05 have been fully considered but they are not persuasive.

A. Applicant contends that Fig. 3 and 6 of the cited reference does not include a lead on the TAB leadframe which extends outward from the electrical component to a perimeter I/O of the IC chip, as recited in claim 7.

However, as explained above, Fig. 7 in Buckley, III, et al. disclose the second IC chip/electrical component (see 94 in Fig. 7) having a smaller area than that of the IC chip being mounted above/below a surface of the IC chip and electrically connected to the IC chip via respective lead pads/leads, which extend outward (24A not being numerically referenced in Fig. 7) from the second IC chip/electrical component to the perimeter bonding pads/I/O pads IC chip (see connections between 94 and 56 through 24A in Fig. 7, 6 and 3; Col. 7, lines 55-67).

B. Applicant contends that the cited reference does not include an electrical component mounted on or above the major surface of the IC chip and electrically connected to the IC chip via at least one lead which has a contact exposed interior to the ILB portion of the TAB structure and above a major surface of the IC chip, as recited in claim 11.

As explained above, Fig. 7 in Buckley, III, et al. disclose the second IC chip/electrical component (see 94 in Fig. 7) being mounted with the configuration which provides the leads/traces/pads wiring being internally routed relative to the ILB area so that the leads have respective contacts/terminals being exposed (contacts on the TABLF under the second component 94 not numerically referenced in Fig. 7- see

similar terminals/contacts under bumps in Fig. 6; also see 76 in Fig. 5) interior to the ILB portion of the TABLF structure above/below the major surface of the IC chip/die.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

09-08-05

Nitin Parekh

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800